

///

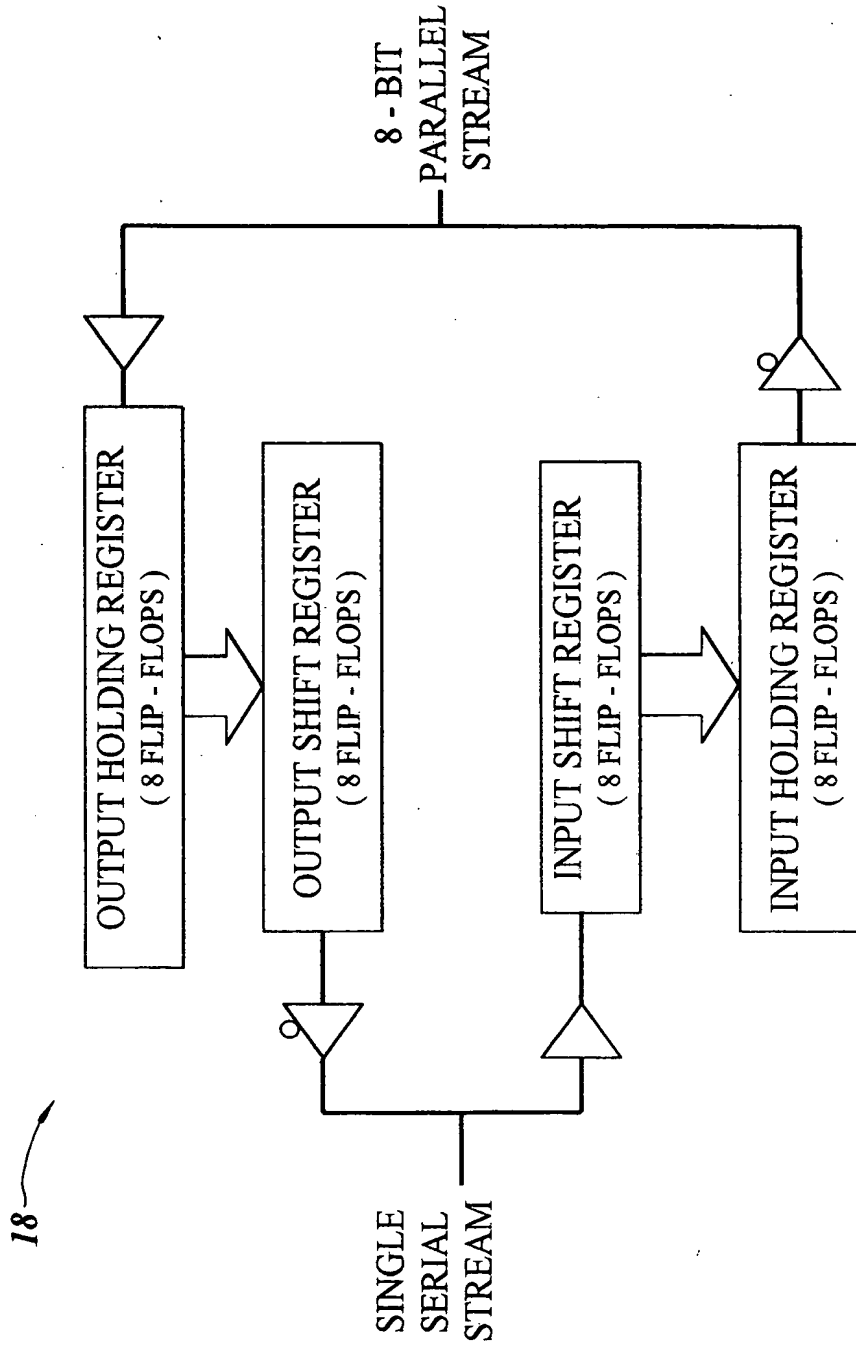


FIG. 1
(PRIOR ART)

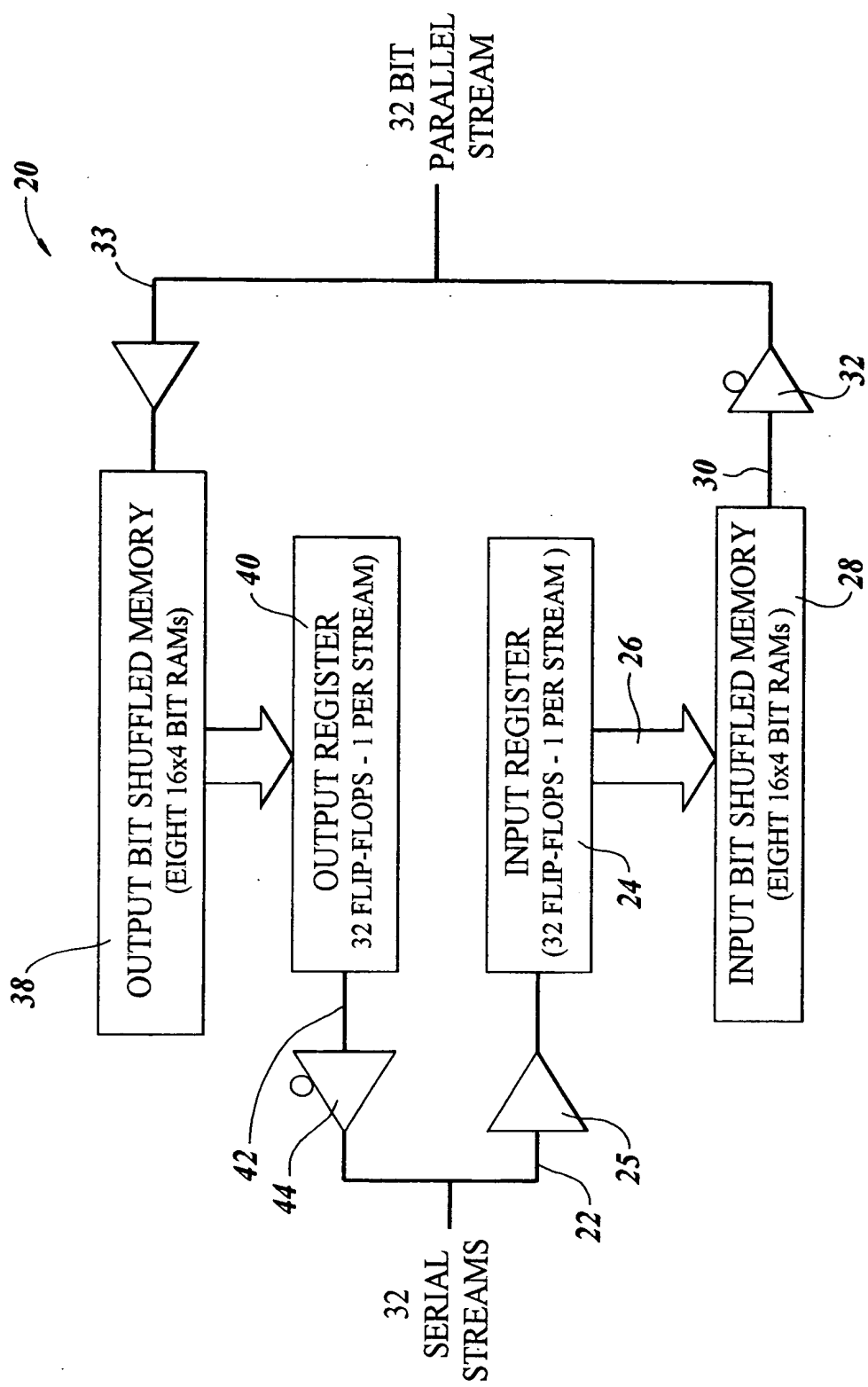


FIG. 2

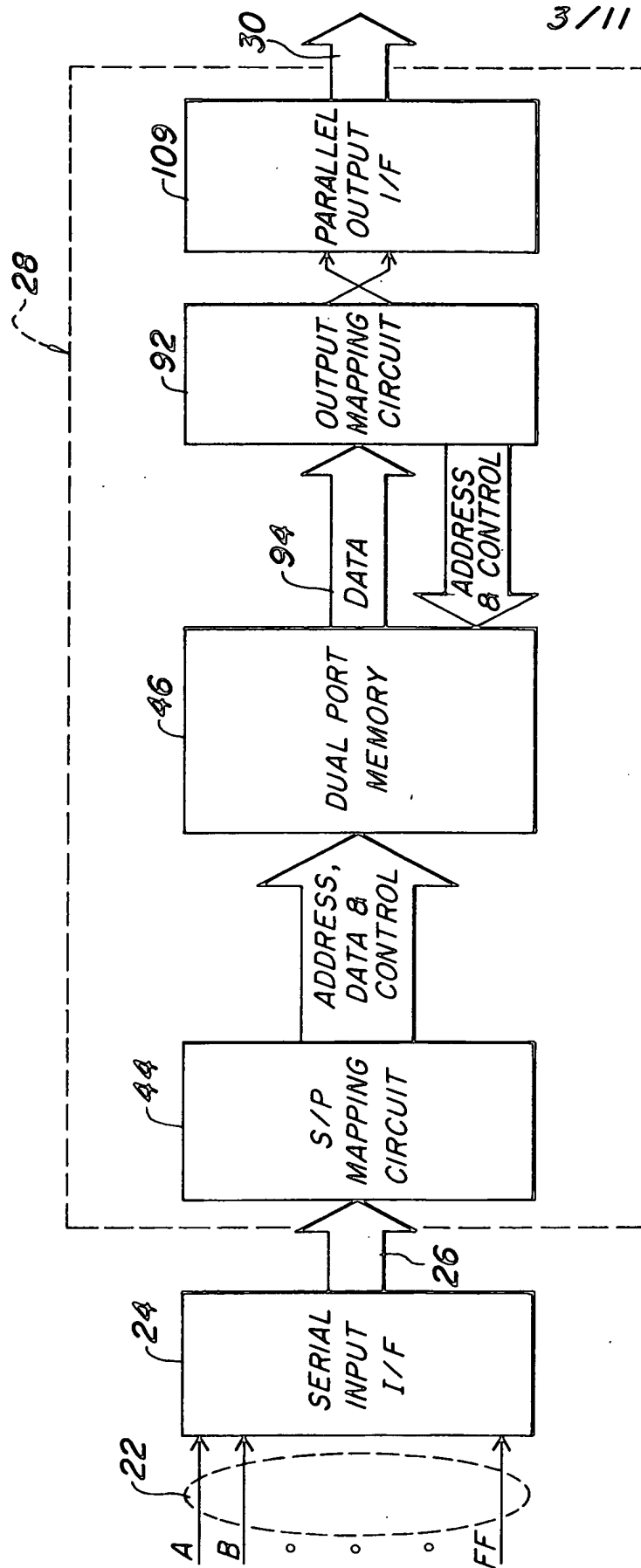


FIG. 3

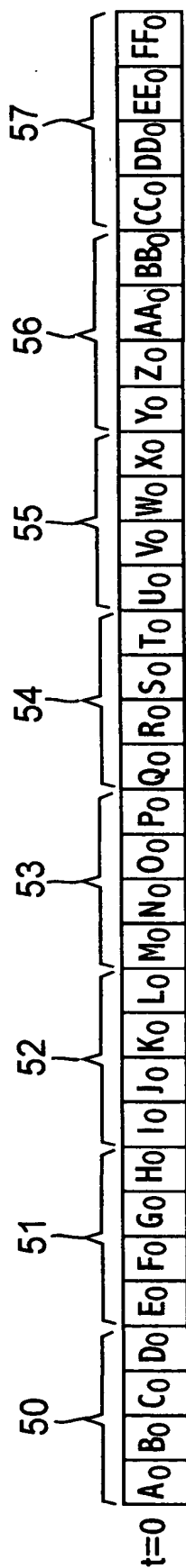


Fig. 4A

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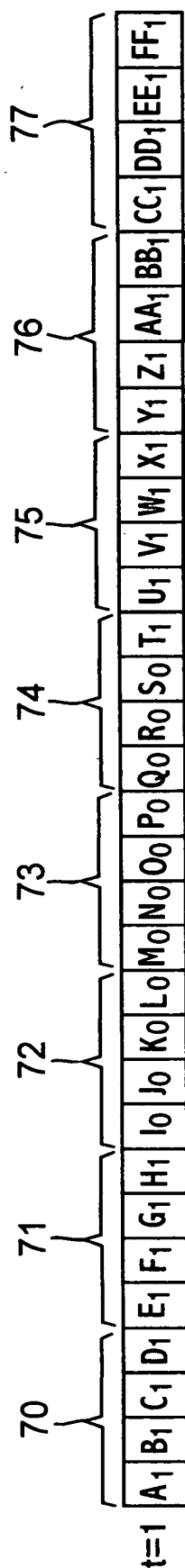


Fig. 4B

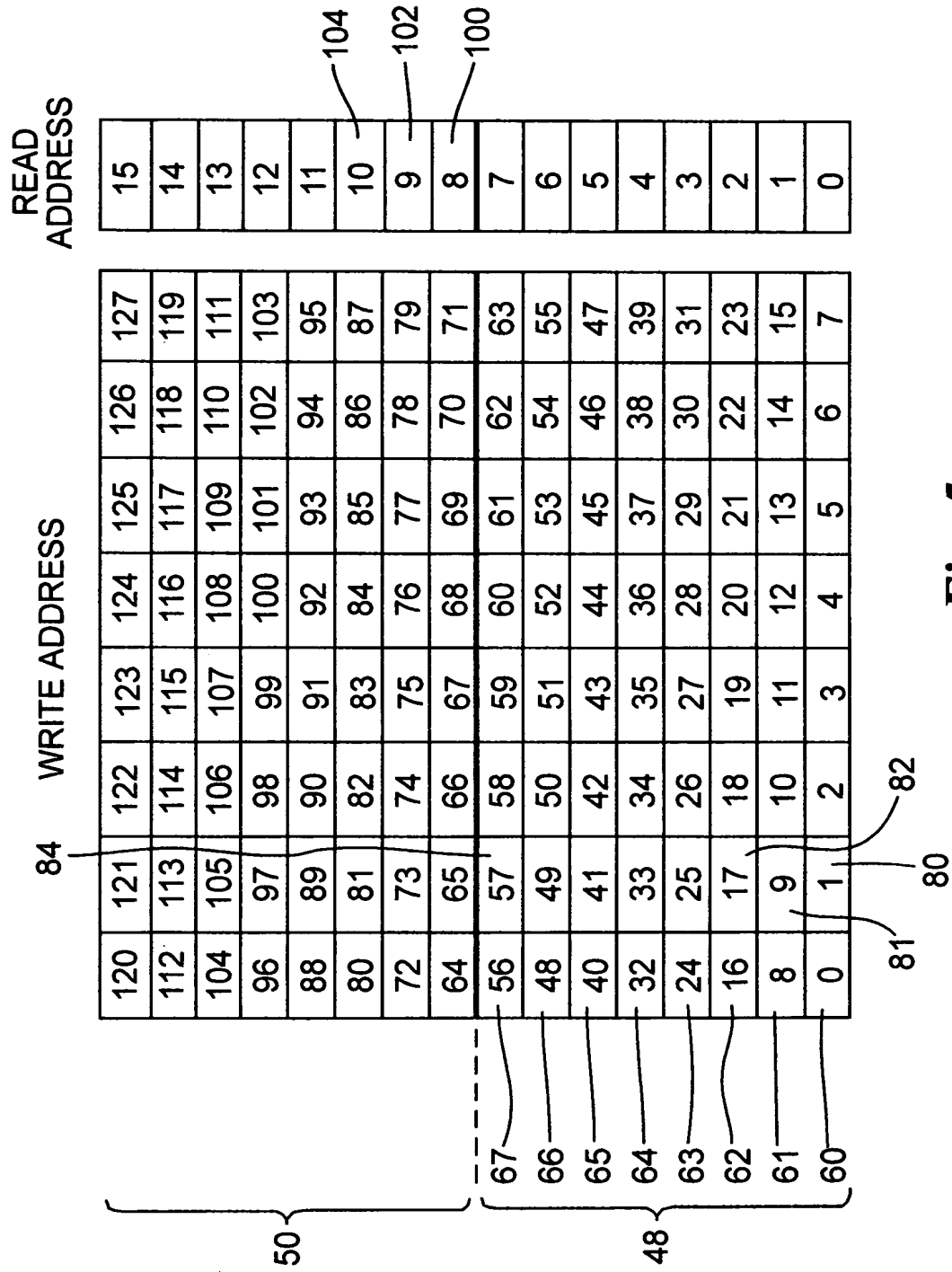
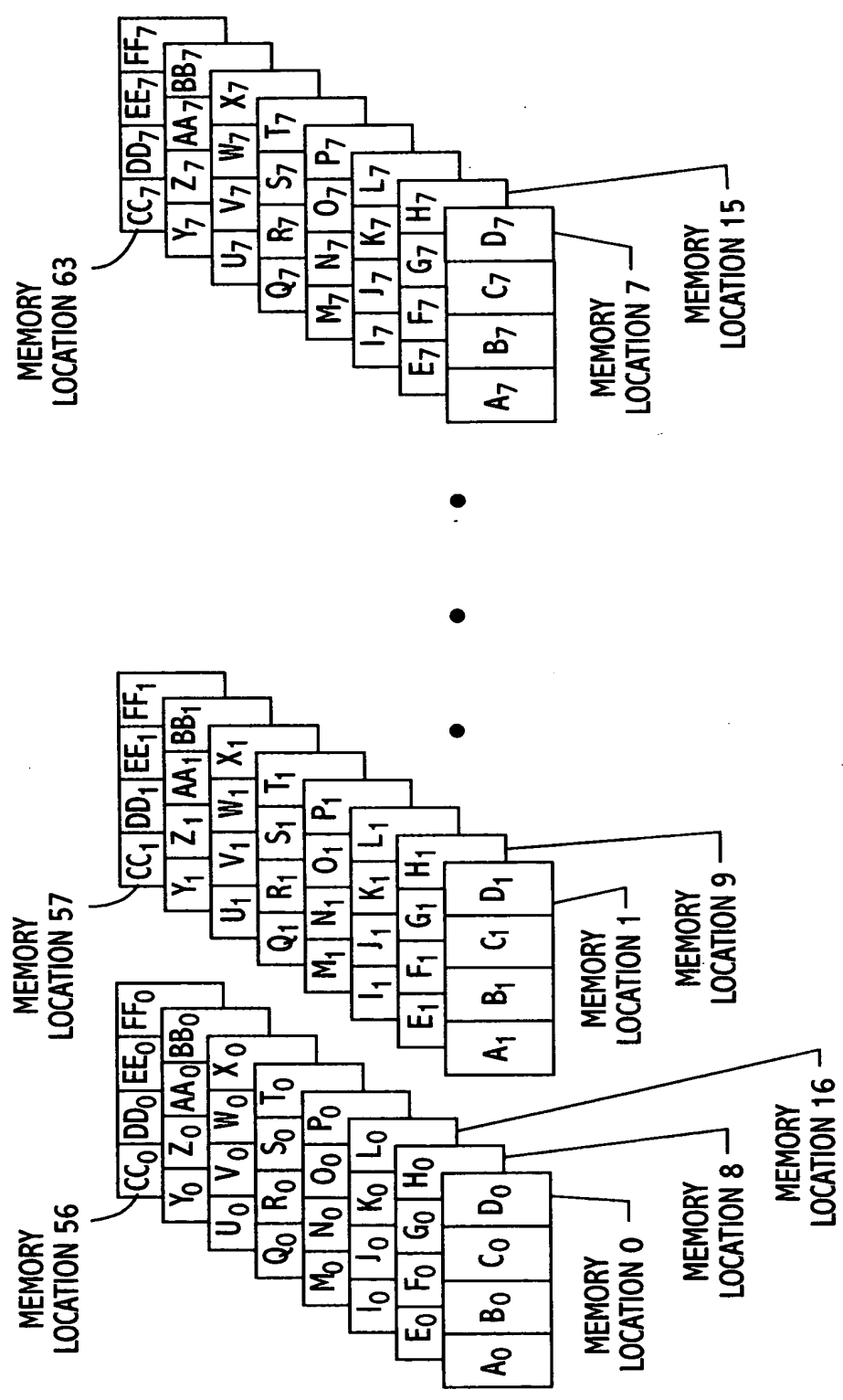


Fig. 5



EIGHTH COLUMN
OF DUAL PORT
MEMORY 46
(DATA FOR $t=7$)

Fig. 6

SECOND COLUMN
OF DUAL PORT
MEMORY 46
(DATA FOR $t=1$)

FIRST COLUMN
DUAL PORT
MEMORY 46
(DATA FOR $t=0$)

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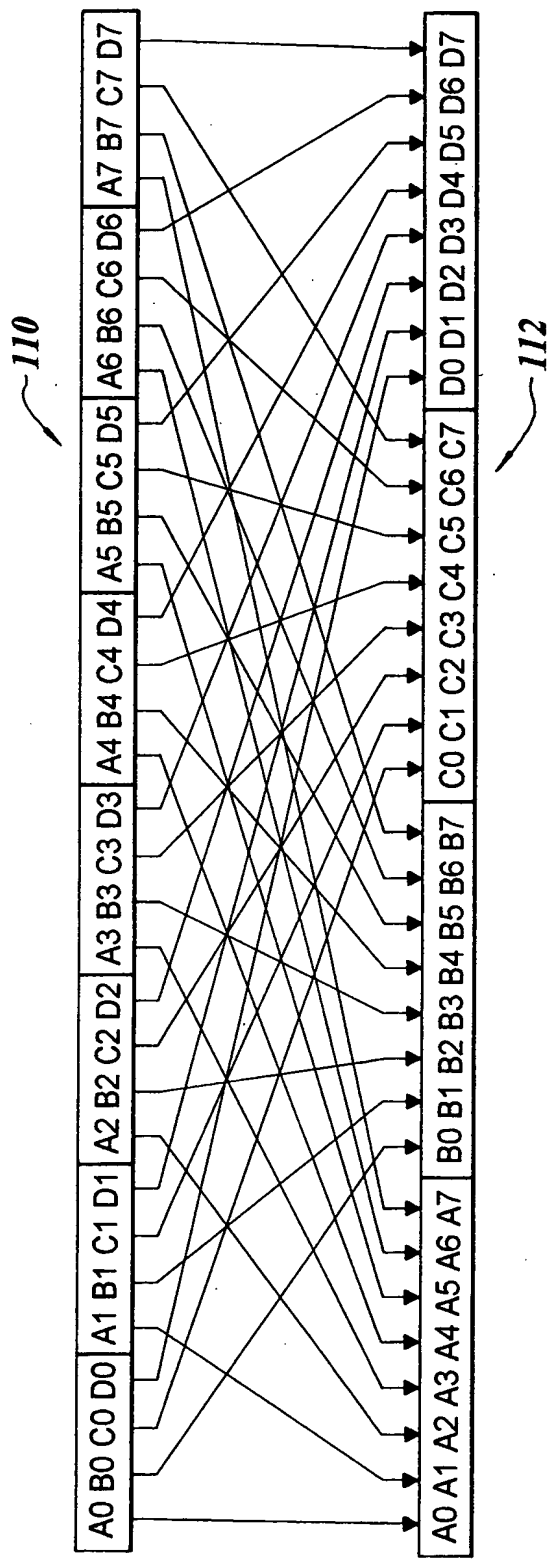


FIG. 7

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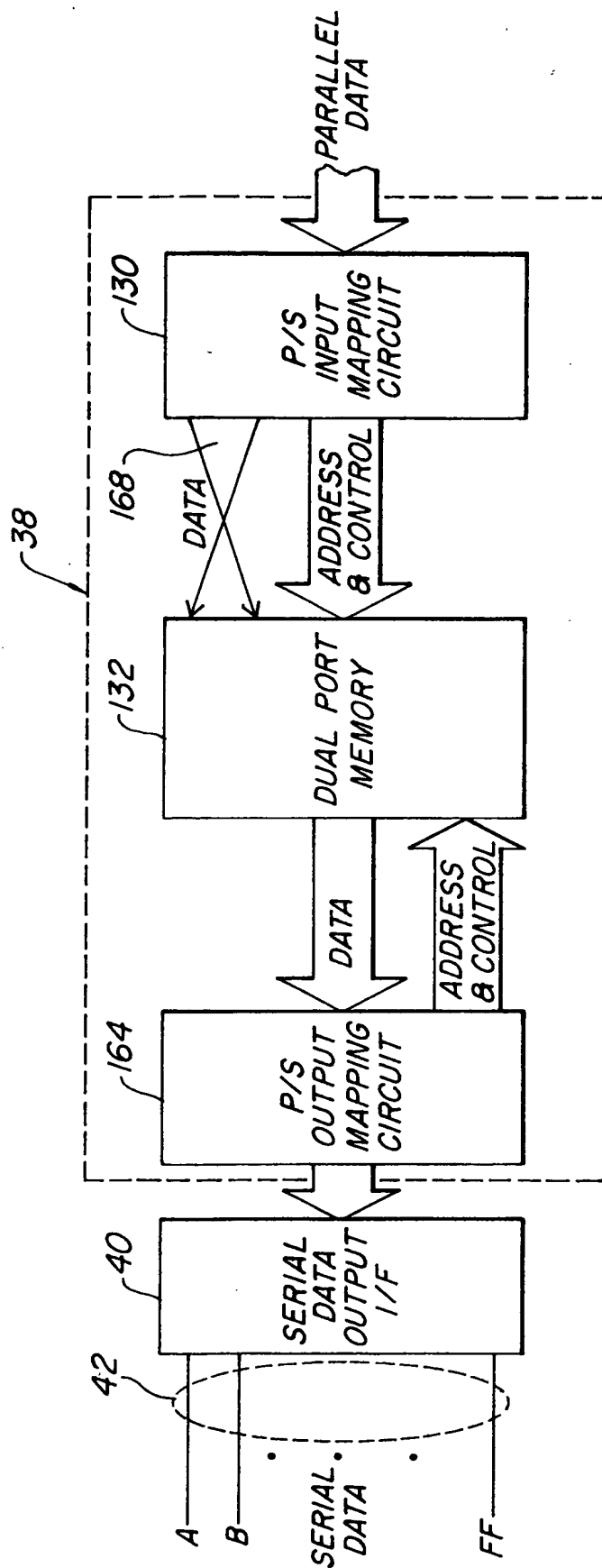


FIG. 8

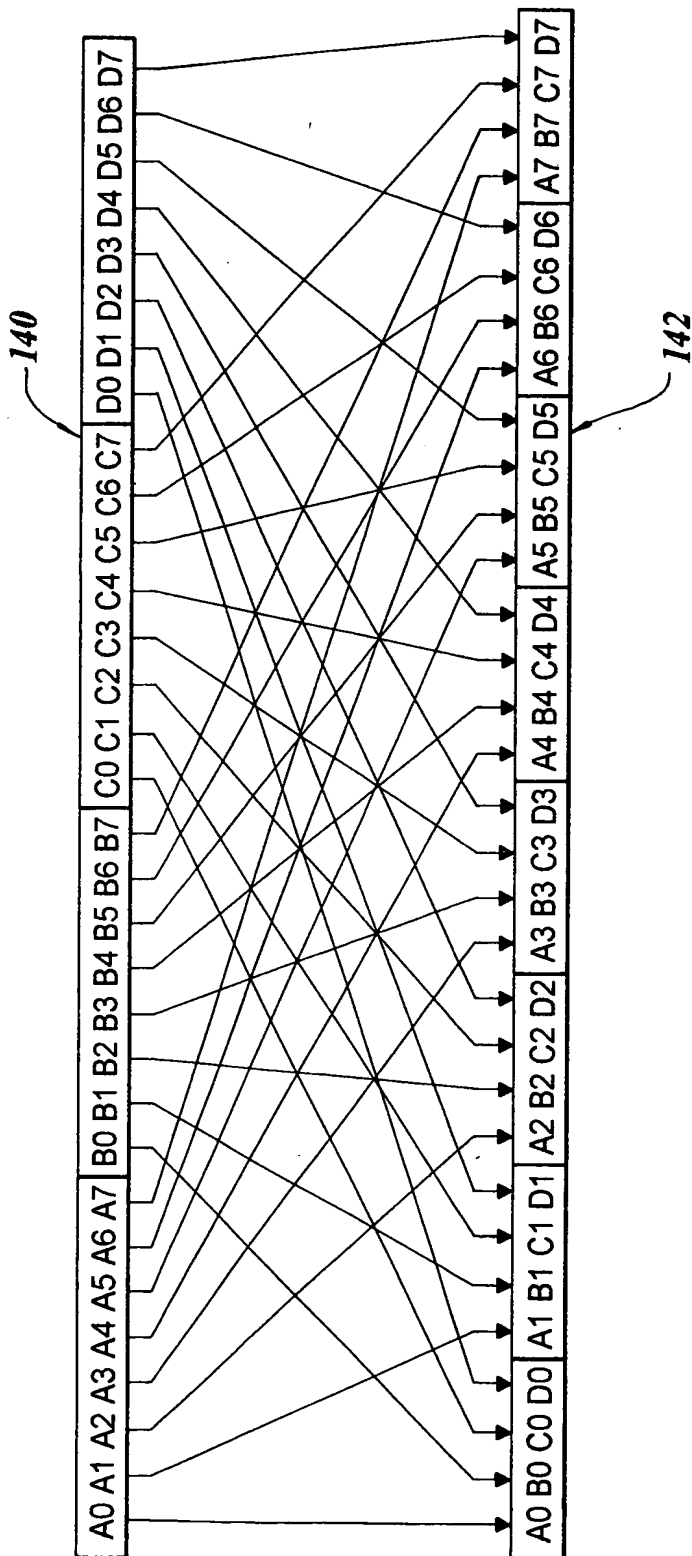


FIG. 9



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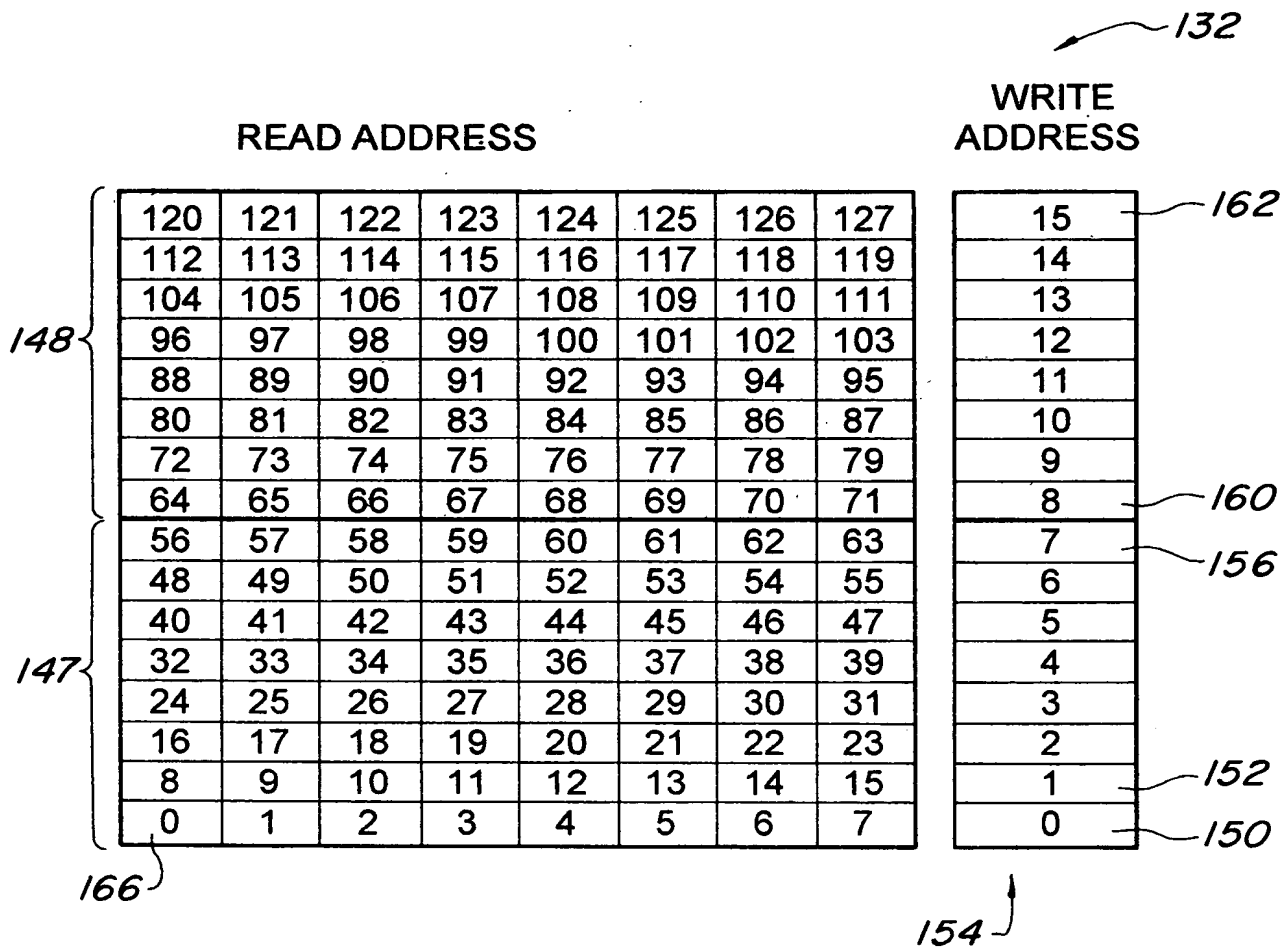


FIG. 10



180

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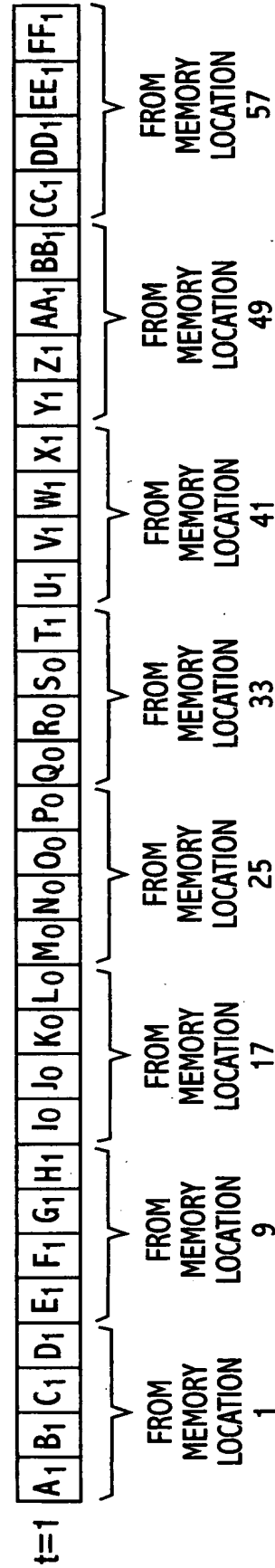
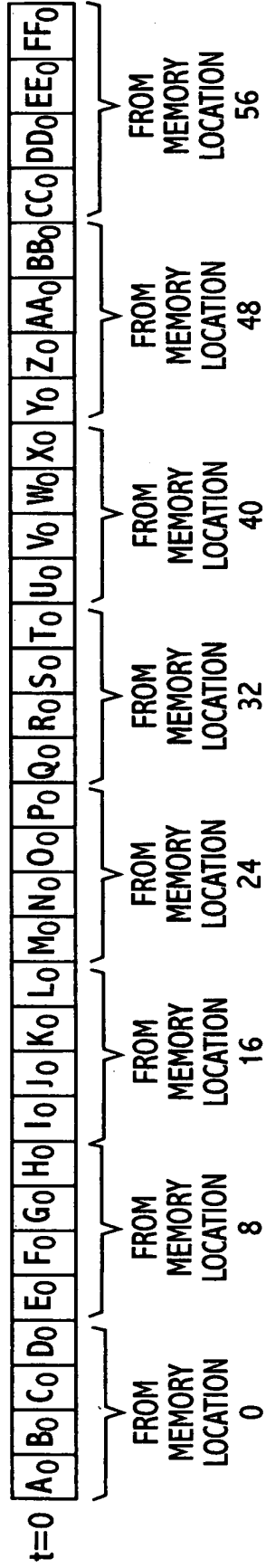


Fig. 11